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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,260	06/29/2004	Han-Sheng Lee	DP-300108	4259

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EXAMINER
BOOSALIS, FANI POLYZOS

ART UNIT	PAPER NUMBER
2884	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,260	LEE ET AL.	
	Examiner	Art Unit	
	Faye Boosalis	2884	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 6-9, 14-15 and 17-18 are rejected under 35 U.S.C. 102(b) as being anticipated by *Jack et al (US 5,689,087 A).*

Regarding claim 1, Jack discloses an optical sensor package comprising: a substrate (12) in which a cavity (26) is defined, a second surface opposite the first surface (12), and a wall (28) between the cavity (26) and the second surface, at least a portion of the substrate being formed of silicon; a membrane (14) bonded to the substrate and spanning the cavity (26) in the substrate; an optical sensing element (20) (22) (24) on the membrane; and a window (30) at the second surface for enabling infrared radiation passing through the wall (28) of the substrate to pass therethrough to the optical sensing element (20) (22) (24), the wall allowing only radiation of wavelengths longer than 1.1 micrometers (i.e. thermal infrared band) to pass therethrough to the optical sensing element (See Fig. 1d and col. 3, lines 1-67, col. 4, lines 1-5, lines 36-50, lines 56-67 and col. 5, lines 1-4 and lines 10-14).

Regarding claim 2, Jack discloses the optical sensor package wherein the optical sensing element is a thermopile (20) (22) (24) (See Fig. 1d and Abstract).

Regarding claim 3, Jack discloses the optical sensor package further comprising integrated circuitry on the substrate, the integrated circuitry performing logic functions and signal processing for the optical sensing element (20) (22) (24) (col. 8, lines 59-67 and col. 9, lines 1-4).

Regarding claim 4, Jack discloses the integrated circuitry (16) is between the membrane (14) and the substrate (12) (See Fig. 1d and col. 5, lines 10-14).

Regarding claims 6-8, Jack discloses sensor package further comprising a filtering material (80), epitaxially grown on the second surface of the substrate (82) (col. 8, lines 1-6).

Regarding claim 9, Jack discloses an optical sensor wherein the filtering material (30) is a first chip that constitutes a first portion of the substrate (12), the cavity (26) is defined in a silicon chip that constitutes a second portion of the substrate (12), and the first and silicon chips are bonded together to form the substrate (See Fig. 1d).

Regarding claim 14, Jack discloses an infrared sensor package comprising: a substrate (12) having a first surface in which a cavity (26) is defined, a second surface opposite the first surface (12), and a wall (28) defined between the cavity (26) and the second surface, at least a portion of the substrate being formed of silicon; a membrane (14) bonded to the substrate and spanning the cavity (26) in the substrate (12); a thermopile sensing element (20) (22) (24) on the membrane (14); and integrated circuitry (16) on the substrate, the integrated circuitry performing logic functions and signal processing for the thermopile sensing element (20) (22) (24); a window (30) at the second surface for enabling infrared radiation to pass through the wall (28) of the

substrate (12) to the thermopile sensing element (20) (22) (24) (See Fig. 1d and col. 3, lines 1-67, col. 4, lines 1-5, lines 36-50, lines 56-67 and col. 5, lines 1-4 and lines 10-14).

Regarding claim 15, Jack discloses the infrared sensor package wherein the wall (28) is defined by the silicon portion of the substrate (12) (See Fig. 1d).

Regarding claims 17-18, Jack discloses infrared sensor package further comprising a filtering material (80), epitaxially grown on the second surface of the substrate (82) (col. 8, lines 1-6).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Jack et al (US 5,689,087 A)* as applied to claim 1 above, and further in view of *Liddiard et al (US 5,369,280 A).*

Regarding claim 5, Jack discloses an optical sensor package comprising: a substrate (12) in which a cavity (26) is defined, a second surface opposite the first surface (12), and a wall (28) between the cavity (26) and the second surface, at least a portion of the substrate being formed of silicon; a membrane (14) bonded to the substrate and spanning the cavity (26) in the substrate; an optical sensing element (20) (22) (24) on the membrane; and a window (30) at the second surface for enabling

infrared radiation passing through the wall (28) of the substrate to pass therethrough to the optical sensing element (20) (22) (24), the wall allowing only radiation of wavelengths longer than 1.1 micrometers (i.e. thermal infrared band) to pass therethrough to the optical sensing element (See Fig. 1d and col. 3, lines 1-67, col. 4, lines 1-5, lines 36-50, lines 56-67 and col. 5, lines 1-4 and lines 10-14). Jack does not disclose a monocyrstallographic silicon chip. Liddiard discloses a thermal infrared detector wherein a substrate (6) and a wall (filter) are defined by a monocrystallographic silicon chip (col. 2, lines 57-67 and col. 5, lines 1-18). Liddiard teaches a single detector, or a two-dimensional planar array of detectors, may be prepared by monolithic microcircuit processing techniques on a monocrystalline silicon substrate, and integrated with associated microelectronic signal conditioning and multiplexing circuits fabricated on the same substrate. When employed with a suitable optical system, the detector or detector array detects infrared heat radiation emitted from bodies within the field of view of the optical system (col. 2, lines 3-12). Therefore, it would have been obvious to modify the infrared sensor package disclosed by Jack, to include a monocrystalline silicon chip, as disclosed supra by Liddiard, to allow for a more versatile sensor package.

Regarding claim 11, Liddiard discloses the optical sensor package further comprising an antireflection coating on the second surface of the substrate (6), the antireflection coating minimizing reflection of infrared radiation by the substrate (col. 3, lines 1-7 and col. 6, lines 56-58).

Regarding claim 12, Liddiard discloses the window comprising a coating on the antireflection coating, the coating being substantially opaque to infrared radiation and having an opening aligned with the wall of the substrate (6) and the optical sensing elements (3) on the membrane (5) (i.e. pellicle) (col. 3, lines 1-7 and col. 6, lines 54-58).

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Jack et al (US 5,689,087 A)* and *Liddiard et al (US 5,369,280 A)* as applied to claim 6 above, and further in view of *Kern et al (US 6,222,111 B1).*

Regarding claim 10, Jack discloses sensor package further comprising a filtering material (80), epitaxially grown on the second surface of the substrate (82) (col. 8, lines 1-6). Neither Jack nor Liddiard disclose type of filtering materials. Kern discloses a thermopile radiation detector wherein the filtering material consists of germanium (See Abstract). Kern teaches in forming the detector, the filter can be deposited on a layer of backing material such as aluminum foil. Examples of suitable filter materials include alternating layers of zinc selenide/magnesium fluoride or germanium/magnesium fluoride. After the filter is deposited, the backing is removed and suitable thermocouples, such as bismuth/antimony, are deposited on one side of the filter. Incident radiation may be then directed to the reverse side of the filter for selective absorption and detection (col. 3, lines 3-11)., Therefore, it would have been obvious to modify the sensor package disclosed by Jack and Liddiard, to include filtering material consisting germanium, as disclosed supra by Kern, to allow for a more versatile apparatus.

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Jack et al (US 5,689,087 A)* as applied to claim 1 above, and further in view of *Hoffman et al (US 6,603,183 B1)*.

Regarding claim 13, Jack discloses an optical sensor package comprising: a substrate (12) in which a cavity (26) is defined, a second surface opposite the first surface (12), and a wall (28) between the cavity (26) and the second surface, at least a portion of the substrate being formed of silicon; a membrane (14) bonded to the substrate and spanning the cavity (26) in the substrate; an optical sensing element (20) (22) (24) on the membrane; and a window (30) at the second surface for enabling infrared radiation passing through the wall (28) of the substrate to pass therethrough to the optical sensing element (20) (22) (24), the wall allowing only radiation of wavelengths longer than 1.1 micrometers (i.e. thermal infrared band) to pass therethrough to the optical sensing element (See Fig. 1d and col. 3, lines 1-67, col. 4, lines 1-5, lines 36-50, lines 56-67 and col. 5, lines 1-4 and lines 10-14). Jack does not disclose a cap like chip to secure the substrate. Hoffman discloses an imaging sensor package comprising a capping chip (130) (col. 2, lines 30-33, col.6, lines 17-26). Hoffman teaches it is well known in the art for image sensors to include an active area, which is responsive to electromagnetic radiation and image sensors incorporated in an image sensor package to protect image sensors from dust and moisture (col. 1, lines 7-9). Therefore, it would have been obvious to modify the sensor package disclosed by Jack, to include a capping chip, as disclosed supra by Hoffman, to allow for a more versatile optical sensor package.

7. Claims 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Jack et al (US 5,689,087 A)* as applied to claim 14 above, and further in view of *Liddiard et al (US 5,369,280 A).*

Regarding claim 16, Jack discloses an infrared sensor package comprising: a substrate (12) having a first surface in which a cavity (26) is defined, a second surface opposite the first surface, and a wall (28) defined between the cavity (26) and the second surface (12), at least a portion of the substrate being formed of silicon; a membrane (14) bonded to the substrate and spanning the cavity (26) in the substrate (12); a thermopile sensing element (20) (22) (24) on the membrane (14); and integrated circuitry (16) on the substrate, the integrated circuitry performing logic functions and signal processing for the thermopile sensing element (20) (22) (24); a window (30) at the second surface for enabling infrared radiation to pass through the wall (28) of the substrate (12) to the thermopile sensing element (20) (22) (24) (See Fig. 1d and col. 3, lines 1-67, col. 4, lines 1-5, lines 36-50, lines 56-67 and col. 5, lines 1-4 and lines 10-14). Jack does not disclose a monocyrstallographic silicon chip. Liddiard discloses a thermal infrared detector wherein a substrate (6) and a wall (filter) are defined by a monocrystallographic silicon chip (col. 2, lines 57-67 and col. 5, lines 1-18). Liddiard teaches a single detector, or a two-dimensional planar array of detectors, may be prepared by monolithic microcircuit processing techniques on a monocrystalline silicon substrate, and integrated with associated microelectronic signal conditioning and multiplexing circuits fabricated on the same substrate. When employed with a suitable optical system, the detector or detector array detects infrared heat radiation emitted

from bodies within the field of view of the optical system (col. 2, lines 3-12). Therefore, it would have been obvious to modify the infrared sensor package disclosed by Jack, to include a monocrystalline silicon chip, as disclosed supra by Liddiard, to allow for a more versatile sensor package.

Regarding claim 19, Liddiard discloses the substrate (6) comprising a first chip (i.e. infrared window) of a filtering material bonded to a silicon chip (i.e. monocrystalline silicon substrate) in which the cavity (i.e. pyramidal-shaped cavity) is defined (col. 6, lines 52-61).

8. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Jack et al (US 5,689,087 A)* as applied to claim 14 above, and further in view of *Hoffman et al (US 6,603,183 B1).*

Regarding claim 20, Jack discloses an infrared sensor package comprising: a substrate (12) having a first surface in which a cavity (26) is defined, a second surface opposite the first surface (12), and a wall (28) defined between the cavity (26) and the second surface, at least a portion of the substrate being formed of silicon; a membrane (14) bonded to the substrate and spanning the cavity (26) in the substrate (12); a thermopile sensing element (20) (22) (24) on the membrane (14); and integrated circuitry (16) on the substrate, the integrated circuitry performing logic functions and signal processing for the thermopile sensing element (20) (22) (24); a window (30) at the second surface for enabling infrared radiation to pass through the wall (28) of the substrate (12) to the thermopile sensing element (20) (22) (24) (See Fig. 1d and col. 3, lines 1-67, col. 4, lines 1-5, lines 36-50, lines 56-67 and col. 5, lines 1-4 and lines 10-

14). Jack does not disclose a cap like chip to secure the substrate. Hoffman discloses an imaging sensor package comprising a capping chip (130) (col. 2, lines 30-33, col.6, lines 17-26). Hoffman teaches it is well known in the art for mage sensors to include an active area, which is responsive to electromagnetic radiation and image sensors incorporated in an image sensor package to protect image sensors from dust and moisture (col. 1, lines 7-9). Therefore, it would have been obvious to modify the sensor package disclosed by Jack, to include a capping chip, as disclosed supra by Hoffman, to allow for a more versatile optical sensor package.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Faye Boosalis whose telephone number is 571-272-2447. The examiner can normally be reached on Monday thru Friday from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Porta can be reached on 571-272-2444. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

FB

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